AMENDMENTS TO THE SPECIFICATION:

Please replace the first full paragraph on page 15 with the following amended paragraph:

In addition, the NAND gate (NAND_MDU) corresponding to the master delay unit (MDU) receives an input clock (clk_in), a master delay selective signal (MSR), a disable signal (MDU_disz) of the master delay unit. Also, the NAND gates (NAND_SDU 1, NAND_SDU 2, ..., NAND_SDU n-1) respectively corresponding to n-1 slave delay units (SDU 1, SDU 2, ... , SDU n-1) receives the input clock (clk_in), slave delay selective signals (SSR_1, SSR_2, ... , SSR_n-1) and the master delay selective signal ~~(MRS)~~ (MSR).

Please replace the paragraph bridging page 15 and page 16 with the following amended paragraph:

Referring to Fig. 7, each of m sub delay chains (SDC 1, SDC 2, ... , SDC m) includes one master delay unit (MDU) and n-1 slave delay unit (SDU). Herein, the master delay unit (MDU) of each sub delay chain (SDC 1, SDC 2, ... , SDCm) is controlled by m master delay selective signals (MSR_1, ... , MSR_m) outputted from the master shift register 262, respectively. Furthermore, the n-1 slave delay selective signals (SSR_1, SSR_2, ... , SSR_n-1) are inputted to each sub delay chain (SDC 1, SDC 2, ... , SDC m). In short, the master delay unit (MDU) of the first sub delay chain (SDC 1) is controlled by the master delay selective signal ~~(MRS_1)~~

(MSR_1) and the master delay unit (MDU) of the m^{th} sub delay chain (SDC m) is controlled by the m^{th} master delay selective signal ~~(MRS_m)~~ (MSR_R). The other hand, the first slave delay unit (SDU 1) of the first sub delay chain (SDC 1) and the first slave delay unit (SDU 1) of the second sub delay chain (SDC 2) is controlled by the identical slave delay selective signal (SSR_1).